REMARKS

In the Office Action, the Examiner rejected claims 18-29 under 35 U.S.C. §102(e) as being unpatentable over United States Patent Publication 2003/0005399 by Igarashi, et al. ("Igarashi"). The Examiner also rejected claims 19-29 under 35 U.S.C. §102(e) as being unpatentable over United States Patent 6,912,704 to Teig, et al. ("Teig"). In this Amendment, Applicants have amended claim 18. Applicants have canceled claim 19 but have not added any claims. Accordingly, claims 18 and 20-29 will be pending after entry of this Amendment.

I. Rejection under §102(e) over Igarashi

In the Office Action, the Examiner rejected claims 18 and 20-29 under §102(e) as being unpatentable over Igarashi. Claims 20-29 are dependent directly or indirectly on independent claim 18. Claim 18 recites a clock signal distribution network on an integrated circuit (IC) layout, where the clock signal distribution layout has a collection of non Manhattan clock signal lines and a collection of Manhattan clock signal lines arranged to form a mesh. The mesh is formed by repeated convex polygon regions. The mesh defines several convex polygonal regions in the IC layout.

Applicants respectfully submit that Igarashi does not disclose every limitation of claim 18. Specifically, in the Office Action, the Examiner cited paragraphs 0174 and 0176 of Igarashi for disclosing a collection of non Manhattan clock signal lines arranged to form a mesh. Applicants respectfully submit that the cited paragraphs describe the clock distribution tree of Figure 31. As shown in Figure 31, this distribution tree is not a mesh and also does not have Manhattan lines.

Igarashi, in Figures 34-37 does show an integrated circuit that has a clock mesh. See, Igarashi paragraphs 0059-0062. However, Igarashi's mesh only includes non-Manhattan liens. Specifically Igarashi in paragraph 0189 describes the mesh of Figure 34 as: "a clock mesh 520 which is constituted by use of oblique lines and set up approximately all over the chip" [emphasis added]. Similarly, Igarashi in paragraph 0192 describes the mesh of Figure 35 as: "a clock mesh 640 constituted by oblique lines." [emphasis added]. Similarly, Igarashi in paragraph 0196 describes the mesh of Figure 36 as: "a clock mesh 730 which is set up all over the chip; and a plurality of sub-drivers 720 connected to the main clock supply line 712, which drive oblique lines constituting the clock mesh." [emphasis added]. Finally, Igarashi in paragraph 0198 describes the clock mesh of Figure 37 as: "... and a plurality of sub-drivers which drive oblique lines constituting the clock mesh." [emphasis added].

Applicants, therefore, respectfully submit that Igarashi, neither in these figures, nor anywhere else, discloses a signal distribution network that has all limitations of claim 18, namely, a collection of non-Manhattan clock signal lines and a collection of Manhattan clock signal lines arranged to form a mesh that defines several convex polygonal regions in the IC layout.

In view of the foregoing remarks, Applicant respectfully submits that the Igarashi does not make claim 18 unpatentable. Given that claims 19-29 are dependent on claim 18, Applicants respectfully submit that these claims are allowable over Igarashi for at least the same reasons that were provided above for claim 18. In view of the foregoing, Applicant respectfully requests reconsideration and withdrawal of the 102(e) rejection of claims 18 and 20-29 over Igarashi.

II. Rejection under §102(e) over Teig

In the Office Action, the Examiner has rejected claims 18 and 20-29 under §102(e) as being unpatentable over Teig. Claims 20-29 are dependent directly or indirectly on independent claim 18. Claim 18 recites a clock signal distribution network on an integrated circuit layout, where the clock signal distribution layout has a collection of non Manhattan clock signal lines and a collection of Manhattan clock signal lines arranged to form a mesh. The mesh defines several convex polygonal regions in the IC layout.

Applicants respectfully submit that for at least the following two reasons, Teig does not disclose the clock signal distribution network of claim 18. *First*, Teig describes a method for floor planning and placement for integrated circuits. However, a method for floor planning and placement is not a clock signal distribution network. Hence, Teig does not disclose a clock signal distribution of claim 18.

Second, in the Office Action, the Examiner cited Teig, column 12, lines 3-16 as disclosing a collection of non Manhattan clock signal lines arranged to form a mesh. However, the Applicants respectfully submit that the citation describes the difference in cost of wiring two ports in a non Manhattan system with diagonal layers and not a mesh for clock signal distribution.

In view of the foregoing, Applicants respectfully submit that Teig does not render claim 18 unpatentable. As claims 20-29 are dependent directly or indirectly on claim 18, Applicants respectfully submit that claims 20-29 are patentable over Teig for at least the reasons that were discussed above for claim 18. In view of the foregoing, Applicants respectfully request reconsideration and withdrawal of the §102(e) rejection of claims 18 and 20-29 over Teig.

CONCLUSION

In view of the foregoing, it is submitted that all the claims, namely claims 18 and 20-29, are in condition for allowance. Reconsideration of the rejections and objections is requested. Allowance is earnestly solicited at the earliest possible date.

Respectfully submitted,

STATTLER, JOHANSEN & ADELI LLP

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Ali Makoui
Reg. No. 45,536

Stattler Johansen & Adeli LLP
1875 Century Park East, Suite 1360
Century City, CA 90067-2514
Phone: (310)785-0140 x302
Fax: (310)785-9558